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CS 433

Homework 3

1. Problem 8.1

a)Describe exactly how, in general, a virtual address generated by the CPU is translated into a physical main memory address?

* First, the binary address is split into a virtual page number and an offset.
* You use the VPN as an index into the page table.
* Then, use you the VPN to find the page frame number on the same table.
* After you find the page frame number, you combine the page frame number with the offset to get the physical memory address ( VPN \* page size) + offset.

b) What physical address, if any, would each of the following virtual addresses correspond to? (1052, 2221, 5499)

i) For 1052:

* 1052 / 1024 = 1
* 1052%1024 = 28
* From this, the remainder is 28 and the quotient is 1. Go on the page table for processes, and find the virtual page number (1 in our case). Then, go and find the page frame number from that row (7). Multiply 7 by 1024 and add the remainder (28). (7 \* 1024) + 28 = 7196.

ii) For 2221:

* 2221 / 1024 = 2
* 2221%1024 = 173
* From this, the remainder is 173 and the quotient is 2. Go on the page table for processes, and find the virtual page number (-- in our case). On this row in the table, the valid bit is set to 0, and a page fault occurs since on the page frame number, you get a -.

iii) For 5499:

* 5499 / 1024 = 5
* 5499%1024 = 379
* Since the quotient is 5, and the remainder 28, we go to the 6th row on the virtual page number column. Then, we go all the way across to page from number, which is 0. We multiply 0 by 1024 and then add the remainder (379).
* (0 \* 1024) + 379 = 379.

1. Problem 8.4

Consider the following string of pages references (7,0,1,2,0,3,0,4,2,3,0,3,2). Complete a figure similar to Figure 8.14 showing the frame allocation for:

1. FIFO

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1) | 2) | 3) | 4) | 5) | 6) | 7) | 8) | 9) | 10) | 11) | 12) | 13) |
| 7 | 0 | 1 | 2 | 0 | 3 | 0 | 4 | 2 | 3 | 0 | 3 | 2 |
| 7 | 7 | 7 | 2 | 2 | 2 | 2 | 4 | 4 | 4 | 0 | 0 | 0 |
|  | 0 | 0 | 0 | 0 | 3 | 3 | 3 | 2 | 2 | 2 | 2 | 2 |
|  |  | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 3 | 3 | 3 | 3 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |

After being initialized, there are page faults in # 4,6,7,8,9,10,11, for a total of 7.

The miss rate is found by subtracting the page faults from the total number of references, which makes it 6. (13-7)

1. LRU

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1) | 2) | 3) | 4) | 5) | 6) | 7) | 8) | 9) | 10) | 11) | 12) | 13) |
| 7 | 0 | 1 | 2 | 0 | 3 | 0 | 4 | 2 | 3 | 0 | 3 | 2 |
| 7 | 7 | 7 | 2 | 2 | 2 | 2 | 4 | 4 | 4 | 0 | 0 | 0 |
|  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3 | 3 | 3 | 3 |
|  |  | 1 | 1 | 1 | 3 | 3 | 3 | 2 | 2 | 2 | 2 | 2 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |

After being initialized, there are page faults in #4,6,8,9,10,11 for a total of 6.

Miss rate = (13-6) = 7

1. Clock

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1) | 2) | 3) | 4) | 5) | 6) | 7) | 8) | 9) | 10) | 11) | 12) | 13 |
| 7 | 0 | 1 | 2 | 0 | 3 | 0 | 4 | 2 | 3 | 0 | 3 | 2 |
| 7\* | 7\* | 7\* | 2\* | 2\* | 2\* | 2\* | 4\* | 4\* | 4\* | 0\* | 0 | 0 |
|  | 0\* | 0\* | 0 | 0\* | 0\* | 0\* | 0 | 2\* | 2\* | 2 | 2 | 2 |
|  |  | 1\* | 1 | 1 | 3\* | 3\* | 3 | 3 | 3\* | 3 | 3 | 3 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |

After being initialized, there are page faults in #4,6,8,9,11 for a total of 5.

The miss rate = (13-5) = 8

1. Optimal

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1) | 2) | 3) | 4) | 5) | 6) | 7) | 8) | 9) | 10) | 11) | 12) | 13 |
| 7 | 0 | 1 | 2 | 0 | 3 | 0 | 4 | 2 | 3 | 0 | 3 | 2 |
| 7 | 7 | 7 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
|  | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 4 | 4 | 0 | 0 | 0 |
|  |  | 1 | 1 | 1 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |

After being initialized, there are page faults in #4,6,8, and 11, for a total of 4.

Miss Rate = (13-4) = 9

1. List the total number of page faults and miss rate for each policy. Count page faults only after all frames have been initialized.
2. Problem 8.5

A process references five pages: A,B,C,D, and E in the following order:

A;B;C;D;A;B;E;A;B;C;D;E

Assume the replacement algorithm is first in first out and find the number of page transfers during this sequence of references starting with an empty main memory with three page frames. Repeat for four page frames.

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | A | B | E | A | B | C | D | E |
| A | A | A | B | C | D | A | A | A | B | E | E |
|  | B | B | C | D | A | B | B | B | E | C | C |
|  |  | C | D | A | B | E | E | E | C | D | D |

3 1 1 1 1 0 0 1 1 0

3+1+1+1+1+1+1 = 9 transfers for three page frames

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | A | B | E | A | B | C | D | E |
| A | A | A | A | A | A | B | C | D | E | A | B |
|  | B | B | B | B | B | C | D | E | A | B | C |
|  |  | C | C | C | C | D | E | A | B | C | D |
|  |  |  | D | D | D | E | A | B | C | D | E |

4 0 0 1 1 1 1 1 1

4 + 1 + 1 + 1+ 1 + 1 + 1 = 10 transfers

1. Problem 8.6

LRU:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 21 | 32 | 33 |
| 1 | 0 | 2 | 2 | 1 | 7 | 6 | 7 | 0 | 1 | 2 | 0 | 3 | 0 | 4 | 5 | 1 | 5 | 2 | 4 | 5 | 6 | 7 | 6 | 7 | 2 | 4 | 2 | 7 | 3 | 3 | 2 | 3 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
|  | 0 | 0 | 0 | 0 | 0 | 6 | 6 | 6 | 6 | 2 | 2 | 2 | 2 | 2 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
|  |  | 2 | 2 | 2 | 2 | 2 | 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 2 | 2 | 2 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
|  |  |  |  |  | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 3 | 3 | 3 | 3 | 1 | 1 | 1 | 1 | 1 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 3 | 3 | 3 | 3 |
|  |  |  |  |  |  | F |  | F |  | F |  | F |  | F | F | F |  | F |  |  | F | F |  |  | F | F |  |  | F |  |  |  |

Number of page faults = 13

Hit ratio = # page faults / total page references = (13/33) = .39 = 39%

b) FIFO

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 21 | 32 | 33 |
| 1 | 0 | 2 | 2 | 1 | 7 | 6 | 7 | 0 | 1 | 2 | 0 | 3 | 0 | 4 | 5 | 1 | 5 | 2 | 4 | 5 | 6 | 7 | 6 | 7 | 2 | 4 | 2 | 7 | 3 | 3 | 2 | 3 |
| 1 | 1 | 1 | 1 | 1 | 1 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 2 | 2 |
|  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
|  |  | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
|  |  |  |  |  | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 3 | 3 | 3 | 3 | 3 | 3 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 3 | 3 | 3 | 3 |
|  |  |  |  |  |  | F |  |  | F |  | F | F |  | F | F | F |  | F |  |  | F | F |  |  |  | F |  |  | F |  | F |  |

Number of page faults = 13

Hit ratio = # page faults / total page references = (13/33) = .33 = 39%

For LRU, the hit ratio is 39% and for FIFO, the hit ratio is 39% as well, meaning that each of these two policies have the same effective performance.